Claims

1. A hetero-interface field effect transistor comprising:

a substrate; and

a cation-polarity layered structure including at least a barrier layer and a channel layer wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0 \leq x \leq 0.30$.

2. The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_{0.17}Al_{0.83}N$

3. The hetero-interface field-effect transistor according to claim 2 wherein said channel layer includes GaN

4. The hetero-interface field-effect transistor according to claim 2 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range of about $0<y\leq 1$.

5. The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0 \leq x<0.17$.

6. The hetero-interface field-effect transistor according to claim 5 wherein said channel layer includes GaN

7. The hetero-interface field-effect transistor according to claim 5 wherein said channel layer includes $In_yGa_{1-y}N$ ($0<y\leq 1$).

8. The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0.17<x\leq 0.25$

9. The hetero-interface field-effect transistor according to claim 8 wherein said channel layer includes GaN.

10. The hetero-interface field-effect transistor according to claim 8 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range of about $0<y\leq 1$.

11. The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0.25<x\leq 0.30$.

12. The hetero-interface field-effect transistor according to claim 11 wherein said channel layer includes $In_yGa_{1-y}N$, x being in the range of about $0<y\leq 1$.

13. A hetero-interface field effect transistor comprising:

a substrate; and

a layered QW structure including at least a barrier layer and a channel layer providing the total two dimensional electron gas density of above $n_{total} = 1.1 \times 10^{13}$ cm^{-2}.

14. A portable telephone phone comprising the hetero-interface field effect transistor of claim 1 or 13.

15. A communication system comprising the hetero-interface field effect transistor of claim 1 or 13.

16. A low noise amplifier comprising the hetero-interface field effect transistor of claim 1 or 13.

17. A radar system comprising the hetero-interface field effect transistor of claim 1 or 13.

18. A sensor comprising the hetero-interface field effect transistor of claim 1 or 13.

19. An intermediate frequency amplifier comprising the hetero-interface field effect transistor of claim 1 or 13.

20. A direct broadcast satellite system comprising the hetero-interface field effect transistor of claim 1 or 13.

21. A satelite communication system comprising the hetero-interface field effect transistor of claim 1 or 13.

22. A method for fabricating a hetero-interface field effect transistor comprising:

providing a substrate; and

fabricating a layered QW structure including at least a barrier layer and a channel layer providing the total two dimensional electron gas density of above $n_{total} = 1.1 \times 10^{13} cm^{-2}$.

23. A method for fabricating a hetero-interface field effect transistor comprising:

providing a substrate; and

fabricating a layered QW structure including at least a barrier layer and a channel layer wherein barrier layer includes $In_xAl_{1-x}N$ where $0 \leq x \leq 0.30$.

24. A method using a hetero-interface field effect transistor in a communications system comprising:

(a) fabricating the hetero-interface field effect transistor using the steps of:

providing a substrate; and

fabricating a layered QW structure including at least a barrier layer and a channel layer wherein barrier layer includes $In_xAl_{1-x}N$ where $0 \leq x \leq 0.30$; and

(b) using the fabricated hetero-interface field effect transistor in the communications system.

25. A method using a hetero-interface field effect transistor in an electronic device comprising an electronic circuit including a hetero-interface field effect transistor using having a substrate; and a layered quantum well structure including at least a barrier layer and a channel layer providing a polarization-induced charge.

26. An electronic device utilizing a hetero-interface field effect transistor comprising a substrate, and a layered quantum well structure including at least a barrier layer and a channel layer providing a polarization-induced charge.

27. The hetero-interface field-effect transistor according to claim 26 wherein said channel layer includes GaN.

28. The hetero-interface field-effect transistor according to claim 26 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range of about $0<y\leq 1$.

29. The hetero-interface field-effect transistor according to claim 26 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0\leq x<0.17$.

30. The hetero-interface field-effect transistor according to claim 29 wherein said channel layer includes GaN.